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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HAYNES AND BOONE, LLP
901 MAIN STREET, SUITE 3100
DALLAS, TX 75202

EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,928	YEO ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/12/06* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The Non-Final Rejection of the last Office action has been withdrawn. However, the new action has been made. This action is non-final rejection.

Claim Objections

2. Claims 21 and 23 are objected to because of the following informalities:

In claim 21, lines 1 and 2, a phrase "a second wafer" should be changed to "the second wafer".

In claim 23, lines 1 and 2, a phrase "a first wafer" should be changed to "the first wafer".

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 9, 11-13, 18 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaguchi et al. (6,221,738) in view of Henley et al. (6,013,563).

Regarding claims 1-3, 9, 11-12, 18 and 20, Sakaguchi (Figs. 4A-4D and "Example 6") discloses a method of fabricating a metal oxide semiconductor field effect

transistor (MOSFET) device on an insulator layer (column 1, lines 6-12 and column 12, lines 9-10), featuring a silicon channel region comprising the steps of: providing a first single-crystal silicon wafer 101 (column 19, line 63) with a surface comprising of a first semiconductor layer 103 of Ge (column 19, lines 63-65) having a first natural lattice constant; forming a second semiconductor layer 102 of single-crystal silicon (column 20, lines 4-6) having a second natural lattice constant on the first semiconductor material 103, the first and second natural lattice constants being different (column 20, lines 23-25) so that a defect or strain gradient is formed at the interface of the second semiconductor layer 102 and the first semiconductor material 103 (column 8, lines 27-30 and column 20, lines 28-30); providing a second silicon wafer 106 (column 20, lines 16-18) comprising a substrate with or without an overlying insulator layer 105 (column 13, lines 60-63); bonding the second semiconductor layer 102' on the second wafer 106, with an insulator in between, resulting in a third wafer comprised of the second wafer 106, the second semiconductor layer 102' and the first wafer 101 (Fig. 4C); performing an external force cleaving procedure (column 20, lines 20-24) at the interface so that the second semiconductor layer 102' is separated from the first semiconductor layer 103 due to cleaving facilitated by the strain gradient/defect produced by a difference in a lattice constant between Si and Ge (column 20, lines 28-30), resulting in a fourth wafer (see Fig. 4D) comprised of the second semiconductor layer 102 and the second wafer 106; and forming a MOSFET device on the fourth wafer (not shown, see column 1, lines 6-12 and column 12, lines 9-10).

Sakaguchi does not disclose that a water jet or pressurized fluid can be used as the external force in performing cleaving procedure.

However, Henley specifically teaches a known process of using fluid jet (i.e., liquid jet or gas jet) or compressed fluid source (i.e., pressurized liquid, pressurized gas) as the external force in performing cleaving procedure (see Fig. 12A and column 9, lines 29-52). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use fluid jet or compressed fluid source as the external force for separating the layers in Sakaguchi's cleaving process because the fluid jet can be adjusted in direction, location, and magnitude to achieve the desired controlled cleaving process, as taught by Henley (column 9, lines 45-52).

Regarding claims 4, 13 and 21, Sakaguchi further discloses that the insulator layer 105 is an silicon oxide (column 14, lines 23-25) and bonding the second wafer 106 comprises bonding an insulator layer 105 on the second wafer 106 (column 13, lines 61-64) to the second semiconductor layer 102' of the first wafer 101 (Fig. 4C).

5. Claims 6-8, 10, 15-17, 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaguchi et al. (6,221,738) in view of Sharma et al. (5,344,524).

Regarding claims 6-7, 15-16 and 23, as discussed in details above, Sakaguchi does disclose the forming of a second semiconductor layer of Si on a first semiconductor layer of Ge, the first and second semiconductor layers have a difference in a lattice constant (column 20, lines 23-25), and have mutually different mechanical

strengths (column 8, lines 27-30). Sakaguchi does not disclose that the first semiconductor layer comprising silicon and germanium.

However, Sharma (Fig. 5) teaches a method for producing SOI substrate, the method comprising: bonding a first silicon wafer on a second silicon wafer, the first silicon wafer having a silicon substrate 20, a relaxed SiGe layer 23 formed thereon (column 4, lines 48-51), and a strained silicon layer 21 formed on the SiGe layer 23 (column 3, lines 58-61); and performing an etching at the interface of the SiGe layer 23 and the Si layer 21 to separate the Si layer 21 from the SiGe layer 23. Accordingly, it would have been obvious to substitute Ge first semiconductor layer of Sakaguchi with the SiGe layer because SiGe would also have a lattice constant different from the lattice constant of the Si second semiconductor layer.

Regarding claims 8, 10, 17 and 19, Sharma further teaches that the first semiconductor material 23 of silicon and germanium alloy is epitaxially grown to a thickness of about 2 microns (column 3, lines 55-59), with a Ge mote fraction of 10% (column 4, lines 48-52), the Si second semiconductor layer 21 is epitaxially grown (column 3, lines 61-64) to a thickness between about 0.01-2 microns (column 4, lines 22-23).

6. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaguchi and Henley as applied to claims 3 and 12 and further in view of King et al. (US. 4,142,925).

Sakaguchi and Henley disclose the insulator layer is a silicon oxide, but does not disclose the insulator layer is a silicon nitride.

However, King (Fig. 2) teaches the forming of an SOI structure, the SOI structure includes an epitaxial silicon layer formed on an insulator layer made of either silicon oxide or silicon nitride (column 2, lines 43-49). Accordingly, it would have been obvious to form the epitaxial silicon layer of Sakaguchi on the insulator layer made of either silicon oxide or silicon nitride because they both function as an isolation layer for preventing the migration on diffusion between the elements, as taught by King (column 2, lines 43-49).

Response to Arguments

7. Applicant argues that Sakaguchi does not suggest that the cleaving occurs due to a difference in lattice constants between layers 102 and 103.

This argument is not persuasive because Sakaguchi teaches in "EXAMPLE 6" a method of separating a first silicon wafer from a second silicon wafer by the application of an external force, whereby the separation takes place at the epitaxial Si/Ge interface. Specifically, Sakaguchi clearly states at column 20, lines 20-30:

"The boned substrate members were separated by the application of an external force, whereby the separation took place at the epitaxial Si/Ge interface.

It is already known that defects are introduced into the interface due to a difference in a lattice constant between Si and Ge ... Because of such a difference in the lattice constant and the introduction of defects, the Si/Ge interface becomes weaker and causes cleavage."

Therefore, in "example 6" of Sakaguchi clearly teaches the cleaving occurring due to a difference in lattice constants between a first layer 103 made of Ge and a second layer 102 made of Si.

In response to Applicant's arguments with respect to Godbey and Sharma, the previous rejections are withdrawn and the new ground of rejection is applied.

Conclusion

This action is made non-final rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562.

Theresa Doan
June 24, 2006.